


DS - 09/21/2006 **ELECTRONIC INFORMATION DISCLOSURE STATEMENT**

Electronic Version v18

Stylesheet Version v18.0

Title of Invention	DUAL SCAN CHAIN DESIGN METHOD AND APPARATUS																																																
<div style="display: flex; justify-content: space-between; align-items: flex-start;"> <div> <p>Application Number : 10/718445</p> <p>Confirmation Number: 9844</p> <p>First Named Applicant: Sandeep Bhatia</p> <p>Attorney Docket Number: CA7035962001</p> <p>Art Unit: 2138</p> <p>Examiner: John J Tabone Jr</p> <p>Search string: (6377912 or 6694464 or 6574762 or 6114892 or 6158032 or 20050015689).pn</p> </div> <div style="text-align: center;">  </div> </div>																																																	
<p>US Patent Documents</p> <p>Note: Applicant is not required to submit a paper copy of cited US Patent Documents</p> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th>init</th> <th>Cite.No.</th> <th>Patent No.</th> <th>Date</th> <th>Patentee</th> <th>Kind</th> <th>Class</th> <th>Subclass</th> </tr> </thead> <tbody> <tr> <td>JJT</td> <td>1</td> <td>6377912</td> <td>2002-04-23</td> <td>Sample et al.</td> <td>B1</td> <td></td> <td></td> </tr> <tr> <td>I</td> <td>2</td> <td>6694464</td> <td>2004-02-17</td> <td>Quayle et al.</td> <td>B1</td> <td></td> <td></td> </tr> <tr> <td>I</td> <td>3</td> <td>6574762</td> <td>2003-06-03</td> <td>Karimi et al.</td> <td>B1</td> <td></td> <td></td> </tr> <tr> <td>V</td> <td>4</td> <td>6114892</td> <td>2000-09-05</td> <td>Jin</td> <td></td> <td></td> <td></td> </tr> <tr> <td>V</td> <td>5</td> <td>6158032</td> <td>2000-12-05</td> <td>Currier et al.</td> <td></td> <td></td> <td></td> </tr> </tbody> </table>		init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass	JJT	1	6377912	2002-04-23	Sample et al.	B1			I	2	6694464	2004-02-17	Quayle et al.	B1			I	3	6574762	2003-06-03	Karimi et al.	B1			V	4	6114892	2000-09-05	Jin				V	5	6158032	2000-12-05	Currier et al.			
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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet

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of

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Complete if Known

Application Number	10/718,445
Filing Date	November 19, 2003
First Named Inventor	Sandeep Bhatia
Art Unit	2138
Examiner Name	John J. Tabone, Jr.
Attorney Docket Number	CA7035962001

NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
JJT	1	BALAKRISHNAN, K. J., et al., "Deterministic Test Vector Decompression in Software Using Linear Operations", Proceedings of the 21st IEEE VLSI Test Symposium, April 27 - May 1, 2003, pp. 225 - 231, IEEE, Los Alamitos, CA, USA.	
	2	BARDELL, P. H. et al., "Build-In-Test for VLSI: Pseudorandom Techniques", 1987, pp. 61-313, John Wiley and Sons, New York, USA.	
	3	BHATIA, S., "Test Compaction by Using Linear-Matrix Driven Scan Chains", Proceedings of the 18 th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, November 3 - 5, 2003, pp. 185 - 190, IEEE, USA.	
	4	BHATIA, S., "Test Compaction in a Parallel Access Scan Environment", Proceedings of the 6 th Asian Test Symposium (ATS '97), November 17 - 19, 1997, pp. 300 -305, IEEE, Los Alamitos, CA, USA.	
	5	HELLEBRAND, S., et al., "Generation of Vector Patterns Through Reseeding of Multiple-Polynomial Linear Feedback Shift Registers", Proceedings of the International Test Conference, 1992, pp. 120 -124, France.	
	6	HSU, F. F. et al., "A Case Study on the Implementation of the Illinois Scan Architecture", Proceedings of the International Test Conference, 2001, pp. 538 - 547, International Test Conference, Washington, D.C., USA.	
	7	KIEFER, G. et al., "Deterministic BIST with Multiple Scan Chains", Proceedings of the International Test Conference, 1998, pp. 1057 - 1064, International Test Conference, Washington, D.C., USA.	
	8	KRISHNA, C.V. et al., "Reducing Test Data Volume Using LFSR Reseeding with Seed Compression", Proceedings of the International Test Conference, 2002, pp. 321 - 330, International Test Conference, Washington, D.C., USA.	
	9	McCLUSKEY, E. J., "Test Data Compression", Design & Test of Computers, March - April 2003, pp. 76 - 87, Volume 20, Issue 2, IEEE Computer Society and the IEEE Circuits and Systems Society, USA.	
✓	10	RAJSKI, J. et al., "Embedded Deterministic Test for Low Cost Manufacturing Test", Proceedings of the International Test Conference, 2002, pp. 310 - 310, International Test Conference, Washington, D. C., USA.	

Examiner Signature	/John J. Tabone Jr/ (10/10/2006)	Date Considered	
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